Remarks

Claims 1, 2, 6-11, 13-15, 18 and 19 are pending in the present application. All of claims 1, 2, 6-11, 13-15, 18 and 19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Inamori, Crampton and Cho. In view of the following remarks, reconsideration and withdrawal of these grounds of rejection is requested.

Examiner Interview

The Applicant thanks Examiner Wells for the courtesy of the Interview conducted on April 11, 2005. During the Interview, the Applicant's representative (Darius C. Gambino) and the Examiner discussed the various rejections under Cho, Crampton and Inamori. Examiner Wells agreed that the rejections under Cho and Inamori would be obviated by the arguments made by Applicant's representative (i.e., that neither Cho nor Inamori shows a "feedforward" coupled capacitor). With regard to Crampton, Examiner Wells argued that the capacitor 84 shown in Figure 5 of Crampton is coupled in a "feedforward" manner, and the Applicant's representative disagreed. Accordingly, the present Amendment has been filed.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 2, 6-11, 13-15, 18 and 19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Inamori et al. (U.S. Pat. No. 6,229,370), Crampton (U.S. Pat. No. 5,767,721) or Cho et al. (U.S. Pat. No. 6,496,072). For the reasons set forth below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

The present invention comprises, in one exemplary embodiment, a switch 40 including a series switching transistor 42 and a shunt transistor 46 (See Fig. 3). A signal path 51 couples a Radiofrequency (RF) input port 12 to an RF output port 14. A first control voltage V_{HI} is coupled to the signal path 51 near the input port 12. A second control voltage V is coupled to the series switching transistor 42 at its gate, and to the shunt transistor 46. The shunt transistor 46 is coupled to a feedforward capacitor 48 which assists in enhancing the isolation between input port 12 and output port 14, and improving the harmonic noise rejection of the switch 40.

As is well known to those of ordinary skill in the art, a "feedforward" capacitor, by definition, is coupled to at least two terminals of a transistor (e.g., gate and drain, gate and source). See, U.S. Pat. No. 6,426,525 (attached hereto as Exhibit A) which describes a "feedforward" capacitor as being coupled to "one side of a serpentine gate and the closest drain/source bar of a FET..." at col. 1, lines 21-31.

With reference to Figure 3 of the present application, the feedforward capacitor 48 is coupled to the gate (G) and source (S) of the shunt transistor 46. This allows the source current (i_S) flowing from the source (S) and through the feedforward capacitor 48 to be fed back to the gate (through resistor 50), and thus effect the operation of the shunt transistor 46 by changing the gate-source voltage (V_{GS}) of the shunt transistor 46. This change in V_{GS} of the shunt transistor 46 allows the transistor to handle larger drain-source currents (i.e., i_{DS}) without substantially affecting operation.

The Applicant has attached a document entitled "Microwave FET Tutorial" as Exhibit B to this Amendment, which will make clear the functional differences offered by the present

invention which includes a "feedforward" capacitor. For example, the figure on Page 10 of the Tutorial shows the general relationship between drain-source current (i_{DS}), drain-source voltage (V_{DS}) and gate-source voltage (V_{GS}) in a FET. The figure shows two main areas, the 'linear' region in which the drain-source current (i_{DS}) depends on the drain-source voltage (V_{DS}) and the gate-source voltage (V_{GS}), and the 'saturation' region in which the drain-source current (i_{DS}) depends mainly on the gate-source voltage (V_{GS}). It will be noted that, if the gate-source voltage (V_{GS}) of a FET is held constant (e.g., $V_{GS} = -2$), variations in the drain-source current (i_{DS}) may result in the FET operating outside the 'saturation' region (which is an undesirable result for most circuit designers). However, if the gate-source voltage (V_{GS}) is increased at the same time the drain-source current (i_{DS}) is increased, the FET can maintain operation in the saturation region, regardless of current variations.

The "feedforward" arrangement shown in Figure 3 of the present application allows for the gate-source voltage (V_{GS}) of the shunt transistor 46 to increase at the same time the drain-source current (i_{DS}) is increased, by feeding the drain-source current (i_{DS}) back to the gate of the shunt transistor through the "feedforward" capacitor 48 and the resistor 50. In particular, the increasing current flowing through "feedforward" capacitor 48 and the resistor 50 creates an increasing voltage across the resistor, which in turn, increases the gate-source voltage (V_{GS}) of the shunt transistor 46.

In operation, when the second control voltage V is above the pinchoff voltage (V_p) of the series switching transistor 42 (e.g., V_{p24}), the series switching transistor 42 is turned ON and the shunt transistor is turned OFF. Alternatively, when the second control voltage V is below the

pinchoff voltage of the series switching transistor (V_{p24}) and the first control voltage V_{HI} is greater than V_{p24}, the series switching transistor 42 is turned OFF and the shunt transistor is turned ON. For example, if V_{p24} were 2 Volts, any second control voltage V above 2 Volts would bias series switching transistor 42 ON and bias shunt transistor OFF. Similarly, if the second control voltage V dropped to zero (0) Volts, and V_{HI} were maintained above V_{p24} at all times (e.g., at say 5 Volts), the series switching transistor 42 would be biased OFF and shunt transistor 46 would be biased ON. Thus, both the series switching transistor 42 and the shunt transistor 46 may be controlled by a single control signal (e.g., the second control signal V), an action which could not have been accomplished by the prior art circuit shown in Figure 1 (which includes two control voltages V and V') (emphasis added).

Independent claim 1 presently recites:

> An integrated circuit switch comprising: at least two signal ports coupled by a signal path, the signal path including a channel of at least one series FET; a shunt path coupled to ground and including a channel of a shunt FET; a first control voltage applied to the signal path; and, a second control voltage applied to a gate of the series FET and to a drain/source of the shunt FET, wherein the shunt path includes at least one feedforward capacitor. [emphasis added].

Thus, claim 1 requires a circuit including a "first control voltage" applied to a signal path which includes a "series FET," and a "second control voltage" applied to the gate of the series FET and the source or drain of a "shunt FET." Claim 1 also requires at least one "feedforward capacitor" coupled to the shunt FET. None of Inamori, Crampton or Cho discloses, teaches or suggests such an invention.

Inamori teaches an amplifier including a signal line 74 with input 14 and output 15, and

variable resistors 71-73 (See Fig. 2). A gain control voltage Vc is applied to the sources of variable resistors 72, 73 and to the gate of variable resistor 71. Inamori does not disclose, teach or suggest a "first control voltage" applied to the signal line 74, or a "feedforward capacitor" coupled to a shunt FET.

In response to the Examiner's arguments, the capacitors 2, 3, 10 and 11 are not "feedforward" capacitors. As discussed above, the term "feedforward" has an accepted definition in the art, and the capacitors 2, 3, 10 and 11 clearly do not meet with that definition as they are only coupled to one terminal of the respective transistors 1, 9 (i.e., drain (D) or source (S)), and do not affect the gate-source voltage (V_{GS}) of the transistors 1, 9. The capacitors 2, 3, 10 and 11 shown in Inamori clearly provide isolation, and not any type of feedforward function.

Crampton teaches a switch circuit 56 with an RF input 58 and an RF output 70. The switch circuit 56 also includes depletion mode FETs 64, 80 which are coupled to a control voltage V1. Crampton does not disclose, teach or suggest a "first control voltage" applied to the signal line connecting the RF input 58 to the RF output 70. Additionally, Crampton does not disclose, teach or suggest a "feedforward capacitor" coupled to FET 80. In fact, the only capacitors coupled to FET 80 are isolation/coupling capacitors 74, 84.

In response to the Examiner's arguments, the capacitors 74, 84 are not "feedforward" capacitors. As discussed above, the term "feedforward" has an accepted definition in the art, and the capacitors 74, 84 clearly do not meet with that definition as they are only coupled to one terminal of the respective transistors 64, 80 (i.e., drain (D) or source (S)), and do not affect the gate-source voltage (V_{GS}) of the FET 80. In fact, there is no way the capacitors 74, 84 could

affect the gate-source voltage (V_{GS}) of the FET 80, as neither one is coupled to the gate (G) of the FET (i.e., capacitor 74 is coupled to drain/source terminal of FET 80, and capacitor 84 is coupled between the drain/source terminal of the FET 80 and ground). The capacitors 74, 84 shown in Crampton clearly provide isolation, and not any type of feedforward function.

Cho teaches an amplifier which couples an antenna 110 to a logic controller through an Low Noise Amplifier (LNA) 108. The amplifier includes FETs 201, 202 which are biased by a control signal V_{cont}. Cho does not disclose, teach or suggest a "first control voltage" applied to the signal line connecting the antenna 110 to the logic controller. Cho also does not disclose, teach or suggest a "feedforward capacitor" coupled to FET 202. Again, the only capacitor coupled to the FET 202 is isolation/coupling capacitor 203.

In response to the Examiner's arguments, the capacitor 203 is not a "feedforward" capacitor. As discussed above, the term "feedforward" has an accepted definition in the art, and capacitor 203 clearly does not meet with that definition as it is coupled to one terminal of the respective transistor 202 (i.e., source terminal (S)), and does not affect the gate-source voltage (V_{GS}) of the transistor 202. The capacitor 203 shown in Cho clearly provides isolation, and not any type of feedforward function.

Accordingly, because none of the cited references disclose, teach or suggest a switch circuit including a "first control voltage" applied to a signal path which includes a "series FET," and a "second control voltage" applied to the gate of the series FET and the source or drain of a "shunt FET," where the shunt FET is coupled to a "feedforward capacitor," reconsideration and withdrawal of this ground of rejection with respect to independent claim 1, is respectfully

requested.

Independent claims 2, 8 and 9 have been amended to include similar limitations to those discussed above with reference to claim 1. Therefore, for at least those reasons discussed above with respect to claim 1, reconsideration and withdrawal of this rejection with respect to claims 2, 8-11, 13-15, 18 and 19 is also respectfully requested.

Independent claim 6 included limitations upon filing directed toward "means for enhancing the isolation between the first and second ports, and for improving the harmonic noise rejection of the switch" which are not disclosed, taught or suggested by the cited references (emphasis added). As the Examiner is well aware, 35 U.S.C. § 112, Paragraph Six entitles patent applicants to define claim limitations by 'means plus function' language, and the recited function cannot be disregarded in examination. See, M.P.E.P §§ 2182 ("...the application of a prior art reference to a means or step plus function limitation requires that the prior art element perform the identical function specified in the claim) and 2183 (Establishment of *prima facie* case requires the prior art element: "(A) performs the function specified in the claim..."). Nowhere do Inamori, Crampton or Cho disclose, teach or suggest means for "enhancing isolation" and "improving harmonic noise rejection."

The Examiner argues that "the circuitry disclosed in the instant figures is clearly equivalent to the circuitry of the applied prior art." However, the Examiner has not interpreted claim 6 in the manner appropriate for claims which include 'means plus function' limitations. First, it should be noted that it is not the Applicant's invention which should be assessed in order to determine 'equivalence,' it is the prior art. Accordingly, the Examiner's statement that the

figures of the present application are "equivalent" to prior art circuits is a misinterpretation of the law. Further, it is not only the circuits themselves which must be reviewed in determining equivalence under § 112, Paragraph Six, it is the claimed function as well.

The Patent Office directs Examiners to interpret 'means plus function' limitations to read on only the structures disclosed in the specification and equivalents thereof. See, M.P.E.P. § 2106; In re Donaldson, 16 F.3d 1189, 1193 (Fed. Cir.). Accordingly, the first step for determining the scope of a 'means plus function' limitation is to determine what structure (or structures) in the specification perform the stated function. Id.

When studying the limitation "means for enhancing the isolation between the first and second ports, and for improving the harmonic noise rejection of the switch" of claim 6, the stated functions are clear, enhancing isolation and improving harmonic noise rejection. Turning to Figure 3 of the present application, these functions are performed by the shunt transistor 46, the resistor 50 and the feedforward capacitor 48. Therefore, any circuits which are identical to, or equivalent to; the circuit comprising shunt transistor 46, the resistor 50 and the feedforward capacitor 48 will anticipate this limitation of claim 6.

As discussed in detail above, none of Inamori, Crampton or Cho disclose, teach or suggest a circuit including at least one "feedforward capacitor" coupled to a shunt FET. Moreover, the individual circuits disclosed by Inamori, Crampton or Cho are not 'equivalent' to the circuit comprising shunt transistor 46, the resistor 50 and the feedforward capacitor 48 shown in Figure 3 of the present application.

In order to be 'equivalent', a prior art element (e.g., circuit) must perform the identical

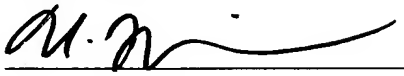
function specified in the claim (emphasis added). The Examiner has failed to identify an element within any of the prior art references which performs the functions of enhancing isolation and improving harmonic noise rejection. For this reason alone, Applicant submits that the Examiner has failed to make out a *prima facie* case of equivalence. See, M.P.E.P. §§ 2183-2184 ("Whether the prior art element performs the identical function specified in the claim..." is a factor, which if not proven by the Examiner, supports a conclusion of non-equivalence).

Additionally, claim 6 has been amended to include a limitation of a "second control signal input" coupled between the first port and the second port. As discussed above with reference to independent claim 1, none of the cited references disclose, teach or suggest a voltage control signal coupled to an RF signal line. Accordingly, reconsideration and withdrawal of this ground of rejection with respect to claims 6 and 7 is respectfully requested.

Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

Respectfully submitted,



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FET STRUCTURES HAVING SYMMETRIC AND/OR DISTRIBUTED FEEDFORWARD CAPACITOR CONNECTIONS

RELATED APPLICATION

The present application claims the benefit of priority based on U.S. Provisional Application No. 60/284,546, filed on Apr. 18, 2001, owned by the assignee of the present invention, and entitled "Symmetric and Distributed Connection of Feedforward Capacitors", which is herein fully incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to field effect transistor (FET) structures and, more particularly, to FET structures having symmetric and/or distributed feedforward capacitor connections.

BACKGROUND OF THE INVENTION

One type of conventional FET structure uses serpentine gates. A feedforward capacitor with a low impedance can be used to improve the harmonic noise rejections of the FETs. By improving the harmonic noise rejections, signal distortions and noise interferences can be reduced or eliminated, and the performance of the FET structures can be improved greatly. To this end, a feedforward capacitor is connected between one side of a serpentine gate and the closest drain/source bar of a FET in a FET structure to improve the harmonic rejection characteristics of the FET structure. FIGS. 1A and 1B are top plan views of two different examples of such conventional serpentine FET structures having conventional feedforward capacitor connections. As shown, a conventional serpentine FET structure **5** or **7** includes a feedforward capacitor **18** and a FET **19** coupled with the feedforward capacitor **18**. The feedforward capacitor **18** includes a bottom metal layer **10**, a dielectric layer (not shown) disposed on the bottom metal layer **10**, and a top metal layer **15** disposed on the dielectric layer. The FET **19** includes a drain manifold **14** having drain fingers **14***a*, a source manifold **16** having source fingers **16***a*, and a serpentine gate **12** serpentining between the drain and source fingers **14***a* and **16***a*.

In the FET structure **5** shown in FIG. 1A, the top metal layer **15** is integrally connected to the drain manifold **14**. That is, the top metal layer **15** functions as the drain manifold **14** of the FET **19** and as the top metal layer of the feedforward capacitor **18**. The serpentine gate **12** of the FET **19** includes one end **12***a* directly connected to the bottom metal layer **10** of the feedforward capacitor **18**, and the other end **12***b* indirectly connected to the feedforward capacitor **18** through the serpentining portion of the gate **12**.

FIG. 1B shows an alternate topology for an FET structure **7** in which the capacitor **18** and the FET **19** are not integrally connected. The capacitor is, however, electrically connected between the capacitor top plate **15** and the FET drain/source manifold **14**. The gate **12** is connected at end **12***a* to the capacitor bottom plate **10**.

Although effective, such conventional serpentine FET structures having the conventional feedforward capacitor connection are somewhat problematic. For example, since only one end of the serpentine gate is directly connected to the feedforward capacitor, the effects of the feedforward capacitor are disproportionately applied across the FET. The end **12***a* of the serpentine gate **12**, which is directly connected to the feedforward capacitor **18**, tends to see the low impedance of the feedforward capacitor **18**, while the other end **12***b* of the serpentine gate **12**, which is not directly connected to the feedforward capacitor **18**, tends to see a much higher impedance. The other end **12***b* experiences a higher impedance because it will experience the impedance of the feedforward capacitor **18** as well as the series gate resistance associated with the serpentine gate **12**. The series gate resistance encountered by the end **12***b* of the serpentine gate **12** reduces or cancels out the positive effect of the feedforward capacitor **18**, such that the benefits of having the feedforward capacitor **18** in the FET structure cannot be effectively realized. Further, since the series gate resistance of the serpentine gate increases as the length of the serpentine gate increases, this problem becomes more significant in large FETs having long serpentine gates.

Accordingly, there is a need for a feedforward capacitor connecting technique for FET structures which overcomes problems associated with conventional feedforward capacitor connecting techniques.

SUMMARY OF THE INVENTION

The present invention provides FET structures which overcome the above-described problems and other problems associated with conventional FET structures. Particularly, in one preferred embodiment, a bussed gate having gate fingers that are directly connected to a feedforward capacitor is used in the FET structure. This distributes evenly or symmetrically the capacitance of the feedforward capacitor to all the gate fingers, so that the effects of the feedforward capacitor can be realized throughout the gate fingers to improve the harmonic rejection characteristics of the FET. Furthermore, since the present invention improves the harmonic noise rejections of the FET structure, the desired linearity in the FET structure can be easily achieved using low control voltages, thereby increasing the efficiency and effectiveness of the FET structure. Thus, the present invention provides a simple technique which effectively solves the problems encountered in prior art FET structures and which is particularly useful in large FET structures having lengthy serpentine gates.

Accordingly, the present invention is directed to a structure comprising a FET including a gate having a plurality of gate fingers, a plurality of source fingers, and a plurality of drain fingers; and a feedforward capacitor integrally coupled with the FET for evenly or symmetrically distributing capacitance of the feedforward capacitor to the gate fingers.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A and 1B are top plan views of two different examples of conventional serpentine FET structures having conventional feedforward capacitor connections.

FIG. 2A is a top plan view of a FET structure according to a first embodiment of the present invention.

FIG. 2B is a cross-sectional view of a feedforward capacitor of the FET structure along line 2B—2B of FIG. 2A according to one embodiment of the present invention.

FIG. 3 is a top plan view of a FET structure according to a second embodiment of the present invention.

FIG. 4 is a top plan view of a FET structure according to a third embodiment of the present invention.

FIG. 5 is a top plan view of a FET structure according to a fourth embodiment of the present invention.

FIG. 6 is a top plan view of a FET structure according to a fifth embodiment of the present invention.

FIG. 7 is a top plan view of a FET structure according to a sixth embodiment of the present invention.

FIG. **8** is a schematic circuit diagram of the structure shown in FIG. **6** or **7** according to one embodiment of the present invention.

FIG. **9** is a top plan view of a FET structure according to a seventh embodiment of the present invention.

FIG. **10** is a top plan view of a FET structure according to an eighth embodiment of the present invention.

FIG. **11** is a top plan view of a FET structure according to a ninth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following embodiments of the present invention are exemplary embodiments and illustrate various structures and methods for feedforward application on single gate devices and multi-gate devices. A 'direct connection' between two components means that there are no other components bridging the two components and that the two components are in contact with each other and extend directly from each other.

FIG. **2A** is a top plan view of a FET structure **100** according to a first embodiment of the present invention, and FIG. **2B** is a cross-sectional view of a feedforward capacitor of the FET structure cut along line **2B—2B** of FIG. **2A** according to one embodiment of the present invention. As shown, the FET structure **100** includes a feedforward capacitor C1 and a serpentine FET **50** integrally coupled with the feedforward capacitor C1. The feedforward capacitor C1 includes a capacitor bottom metal layer **30**, a dielectric layer **21** formed on the bottom metal layer **30**, and a capacitor top metal layer **24** formed on the dielectric layer **21**. The serpentine FET **50** includes the capacitor top metal layer **24** (or a portion thereof) functioning as a drain manifold for providing a plurality of drain fingers **24***a*, a source manifold **26** having a plurality of source fingers **26***a*, and a serpentine gate **31** having a plurality of gate fingers **31***d* serpentining between the drain and source fingers **24***a* and **26***a*.

The serpentine gate **31** includes two end portions **31***a* and **31***b* which are directly connected to the bottom metal layer **30** of the feedforward capacitor C1, and a middle portion **31***c* which is not directly connected to any part of the feedforward capacitor C1. This direct and symmetrical connection of the serpentine gate **31** (i.e., the direction connection of the end portions **31***a* and **31***b* to the metal layer **30**) to the feedforward capacitor C1 allows the feedforward capacitance of the capacitor C1 to be applied symmetrically to both sides of the serpentine gate **31**. No one side of the serpentine gate **31** will be subject to the series gate resistance of the serpentine gate **31**. Instead, both sides of the serpentine gate **31** will benefit equally from the feedforward capacitance of the capacitor C1. This reduces or eliminates signal distortions and improves the linearity and harmonic noise rejection characteristics of the FET structure **100**.

Thus, the present invention improves greatly the performance of the FET structure. Furthermore, since the present invention improves the harmonic noise rejections of the FET structure, the desired linearity in the FET structure can be easily achieved using low control voltages, thereby increasing the efficiency and effectiveness of the FET structure.

FIG. **3** is a top plan view of a FET structure **102** according to a second embodiment of the present invention. As shown, the FET structure **102** includes a feedforward capacitor C1 and a serpentine FET **52** integrally coupled with the feedforward capacitor C1. The FET structure **102** is identical to the FET structure **100** of FIG. **2A**, except that the middle portion **31C** of the serpentine gate **31** as well as the two end portions **31***a* and **31***b* thereof are connected directly to the bottom metal layer **30** of the feedforward capacitor C1. This results in all the gate fingers **31***d* of the serpentine gate **31** being directly connected to the bottom metal layer **30** of the feedforward capacitor C1. This configuration distributes evenly (i.e., in equal or approximately equal amount) and symmetrically the feedforward capacitance of the capacitor C1 across all the gate fingers **31***d* of the serpentine gate **31**, thereby improving significantly the performance characteristics of the FET structure **102**.

FIG. **4** is a top plan view of a FET structure **104** according to a third embodiment of the present invention. As shown, the FET structure **104** includes a feedforward capacitor C1 and a serpentine FET **54** integrally coupled with the feedforward capacitor C1. The FET structure **104** is identical to the FET structure **102** of FIG. **3**, except that the two end portions **31***a* and **31***b* of the serpentine gate **31** are not directly connected to the bottom metal layer **30** of the feedforward capacitor C1. In other words, only the middle portion **31C** of the serpentine gate **31** (and not the two end portions **31***a* and **31***b* of the serpentine gate **31**) is connected directly to the feedforward capacitor C1. This results in the inner gate fingers $31d_2$ and $31d_3$ (and not the outer gate fingers $31d_1$ and $31d_4$) of the serpentine gate **31** to be in direct connection with the feedforward capacitor C1. The manner in which one side (i.e., the fingers $31d_1$ and $31d_2$) of the serpentine gate **31** is connected to the feedforward capacitor C1 is the same as the manner in which the other side (i.e., the fingers $31d_3$ and $31d_4$) of the serpentine gate **31** is connected to the feedforward capacitor C1. Thus, a symmetry in configuration exists between the two sides of the serpentine gate **31**. This configuration symmetrically distributes the feedforward capacitance of the feedforward capacitor C1 to the gate fingers **31***d* of the serpentine gate **31**, and thereby improves the performance characteristics of the FET structure **104**.

In other embodiments, other portion(s) of the serpentine gate **31**, except the two end portions **31***a* and **31***b* of the serpentine gate **31**, can be connected directly to the feedforward capacitor C1 as long as this connection provides symmetry in the connection of the serpentine gate **31** to the feedforward capacitor C1. These configurations distribute symmetrically the feedforward capacitance of the capacitor C1 to the serpentine gate **31**.

FIG. **5** is a top plan view of a FET structure **106** according to a fourth embodiment of the present invention. In this embodiment, instead of having a serpentine FET having a serpentine gate, a bussed FET having a bussed gate is used in a FET structure to connect with a feedforward capacitor. Particularly, as shown, the FET structure **106** includes a feedforward capacitor C1 and a bussed FET **56** integrally coupled with the feedforward capacitor C1. The bussed FET **56** includes a source manifold **26** having source fingers **26***a*, a capacitor bottom metal layer/drain manifold **24** having drain fingers **24***a*, and a bussed gate **32** having bussed gate fingers **32***a* disposed between the drain and source fingers **24***a* and **26***a*. All the gate fingers **32***a* of the bussed gate **32** are directly connected to the bottom metal layer **30** of the feedforward capacitor C1. This allows the feedforward capacitance of the feedforward capacitor C1 to be evenly and symmetrically distributed across all the gate fingers **32***a*, which improves the performance of the FET structure **106** as discussed above.

FIG. **6** is a top plan view of a cascaded FET structure **108** according to a fifth embodiment of the present invention. As shown, the cascaded FET structure **108** includes first, second and third FET structures **100**, **100'** and **100"** that are con-

nected in series with each other. To connect the first FET structure **100** in series with the second FET structure **100'**, a source manifold **260** is used wherein the source manifold **260** has a plurality of first source fingers **260***a* extending in one direction and a plurality of second source fingers **260***b* extending in the opposite direction. To connect the second FET structure **100'** in series with the third FET structure **100"**, a drain manifold **261** is used. The drain manifold **261** has a plurality of first drain fingers **261***a* extending in one direction and a plurality of second drain fingers **261***b* extending in the opposite direction.

The first FET structure **100** is identical to the FET structure shown in FIG. **2**A and includes the feedforward capacitor **C1** and the serpentine FET **50**. The FET **50** includes a serpentine gate **31** having two end portions that are directly connected to the bottom metal layer **30** of the feedforward capacitor **C1**. The first source fingers **260***a* of the source manifold **260** function as the source fingers of the FET **50**. The second FET structure **100'** includes a second FET **50'**. The second FET **50'** includes the second source fingers **260***b* of the source manifold **260** as its source fingers, the second drain fingers **261***b* of the drain manifold **261** as its drain fingers, and a second serpentine gate **31'** serpentining between the source and drain fingers **260***b* and **261***b*.

The third FET structure **100"** includes a third FET **50"** and a second feedforward capacitor **C2** integrally coupled with the third FET **50"**. The second feedforward capacitor **C2** is identical to the first feedforward capacitor **C1**, except that its capacitor top metal layer **24'** functions as the source manifold for providing source fingers **24***a'*. The third FET **50"** includes the source manifold/top metal layer **24'** having the source fingers **24***a'*, the drain manifold **261** having the first drain fingers **261***a*, and a third serpentine gate **31"**. Both ends of the third serpentine gate **31"** are connected directly to the bottom metal layer **30** of the second feedforward capacitor **C2**, which symmetrically distributes the feedforward capacitance of the feedforward capacitor **C2** to the gate fingers of the third serpentine gate **31"**. It should be noted that the FET structure **100"** is basically identical to the FET structure **100**, except that the source and drain sides are switched.

As discussed above, for each of the feedforward capacitors **C1** and **C2**, the two ends of the corresponding serpentine gate are connected directly to the feedforward capacitor **C1** or **C2** whereby the feedforward capacitance effects of the feedforward capacitors **C1** and **C2** are symmetrically applied to the corresponding serpentine gate, thereby greatly improving the performance of the cascaded FET structure **108**.

FIG. **7** is a top plan view of a cascaded FET structure **110** according to a sixth embodiment of the present invention. The cascaded FET structure **110** is identical to the cascaded FET structure **108** shown in FIG. **6**, except that bussed FETs are used in lieu of serpentine FETs on both sides of the cascaded connection. Particularly, as shown in FIG. **7**, the cascaded FET structure **110** includes first, second and third FET structures **106**, **106'** and **106"** that are connected in series with each other. The first FET structure **106** is identical to the FET structure shown in FIG. **5** and includes the feedforward capacitor **C1** and the bussed FET **56**. The FET **56** includes a first bussed gate **32** having bussed gate fingers directly connected to the bottom metal layer **30** of the feedforward capacitor **C1**. The first source fingers **260***a* of the source manifold **260** function as the source fingers of the FET **56**.

The second FET structure **106'** is identical to the second FET structure **100'** in FIG. **6**, and includes a second FET **56'** having a serpentine gate **31'**, second source fingers **260***b*, and second drain fingers **261***b*.

The third FET structure **106"** includes a third FET **56"** and a second feedforward capacitor **C2** integrally coupled with the third FET **56"**. The third FET **56"** includes a source manifold **24'** having source fingers **24***a'*, a drain manifold **261** having first drain fingers **261***a*, and a bussed gate **32"**. All the gate fingers of the bussed gate **32"** are connected directly to the bottom metal layer **30** of the second feedforward capacitor **C2**, which symmetrically and evenly distributes the feedforward capacitance of the feedforward capacitor **C2** to the gate fingers of the bussed gate **32"**. One skilled in the art would note that the third FET structure **106"** is basically identical to the first FET structure **106**, except that the source and drain sides are switched.

For each of the feedforward capacitors **C1** and **C2** in the cascaded FET structure **110**, all the gate fingers of the corresponding bussed gate are connected directly to the feedforward capacitor **C1** or **C2** whereby the feedforward capacitance effects of the feedforward capacitors **C1** and **C2** are evenly and symmetrically distributed to the corresponding bussed gate fingers. This improves greatly the performance characteristics of the cascaded FET structure **110**.

In other embodiments, the FET structures **100** and **100"** of the cascaded FET structure **108** shown in FIG. **6** can be substituted with other FET structures such as the FET structure **102** or **104** shown in FIGS. **3** and **4**. For instance, the FET structures **100** and **100"** can be replaced with two FET structures **102** or two FET structures **104**. In still other embodiments, a mixed combination of the FET structures **100**, **102**, **104** and **106** may be used in one cascaded FET structure. In all these embodiments, any number of FET structures can be cascaded to produce a cascaded FET structure.

FIG. **8** is a schematic circuit diagram of the cascaded FET structure **108** or **110** shown in FIG. **6** or **7** according to one embodiment of the present invention. This circuit diagram clearly indicates that, in the cascaded FET structure **108**, the serpentine gates **31**, **31'** and **31"** respectively correspond to the gates **G1**, **G2** and **G3** in the circuit diagram. The FETs **50**, **50'** and **50"** respectively correspond to the FETs **FET1**, **FET2**, and **FET3**. Similarly, in the cascaded FET structure **110**, the bussed gate **32**, the serpentine gate **31'** and the bussed gate **32"** respectively correspond to the gates **G1**, **G2** and **G3** in the circuit diagram. The FETs **56**, **56'** and **56"** respectively correspond to the FETs **FET1**, **FET2**, and **FET3**.

FIG. **9** is a top plan view of a multi-gate FET structure **112** according to a seventh embodiment of the present invention. As shown, the multi-gate FET structure **112** includes a feedforward capacitor **C1** and a multi-gate FET **57** integrally coupled with the feedforward capacitor **C1**. As discussed above, the feedforward capacitor **C1** includes a capacitor bottom metal layer **30**, a capacitor top metal layer/drain manifold **24**, and a dielectric layer **21** (FIG. **2**B) disposed between the layers **24** and **30**. The multi-gate FET **57** includes the drain manifold **24** having drain fingers **24***a*, a source manifold **26** having source fingers **26***a*, a bussed gate having bussed gate fingers **32***a* directly connected to the capacitor bottom metal layer **30**, and a serpentine gate **33** having serpentine gate fingers **33***a*. The serpentine gate **33** serpentines between the gate fingers **32***a* and the drain or source fingers **24***a* or **26***a*. There exists one bussed gate finger **32***a* and one serpentine gate finger **33***a* between each drain finger **24***a* and an adjacent source finger **26***a*. Since all the gate fingers **32***a* are directly connected to the bottom metal layer **30** of the feedforward capacitor **C1**, the feed-

forward capacitance of the capacitor C1 is evenly and symmetrically distributed to the gate fingers **32***a* of the gate **32**, thereby improving the performance of the FET structure **112**.

FIG. **10** is a top plan view of a multi-gate FET structure **114** according to an eighth embodiment of the present invention. The multi-gate FET structure **114** is identical to the multi-gate FET structure **112** of FIG. **9**, except that the multi-gate FET structure **114** includes an additional serpentine gate **34**. More specifically, as shown, the multi-gate FET structure **114** includes a feedforward capacitor C1 and a multi-gate FET **58** integrally coupled with the feedforward capacitor C1. The multi-gate FET **58** includes a drain manifold **24** having drain fingers **24***a*, a source manifold **26** having source fingers **26***a*, a bussed gate **32** having bussed gate fingers **32***a* directly connected to the capacitor bottom metal layer **30** of the capacitor C1, a first serpentine gate **33**, and a second serpentine gate **34**. The first and second serpentine gates **33** and **34** serpentine between the bussed gate fingers **32***a* and the drain or source fingers **24***a* or **26***a*. The direct connection of all the bussed gate fingers **32***a* to the bottom metal layer **30** of the feedforward capacitor C1 evenly and symmetrically distributes the feedforward capacitance of the capacitor C1 to the gate fingers **32***a*. This improves the performance characteristics of the FET structure **114**.

FIG. **11** is a top plan view of a multi-gate FET structure **116** according to a ninth embodiment of the present invention. In this embodiment, two bussed gates and a serpentine gate are provided. As shown, the multi-gate FET structure **116** includes first and second feedforward capacitors C1 and C3 and a multi-gate FET **59** integrally coupled with the feedforward capacitors C1 and C3. The first feedforward capacitor C1 includes a first capacitor bottom metal layer **30**, a first capacitor top metal layer/drain manifold **24**, and a first dielectric layer disposed between the layers **24** and **30**. The second feedforward capacitor C3 includes a second capacitor bottom metal layer **27**, a second capacitor top metal layer/source manifold **26**, and a second dielectric layer disposed between the layers **26** and **27**.

The multi-gate FET **59** includes the drain manifold **24** having drain fingers **24***a*, the source manifold **26** having source fingers **26***a*, a first bussed gate **32** having first bussed gate fingers **32***a* directly connected to the first capacitor bottom metal layer **30**, a second bussed gate **29** having second bussed gate fingers **29***a* directly connected to the second capacitor bottom metal layer **27**, and at least one serpentine gate **33**. The serpentine gate **33** serpentines between the bussed gate fingers **32***a* and **29***a*. Since all the gate fingers **32***a* are directly connected to the first capacitor bottom metal layer **30** of the first feedforward capacitor C1, and since all the gate fingers **29***a* are directly connected to the second capacitor bottom metal layer **27** of the second feedforward capacitor C3, the feedforward capacitance effects of the capacitors C1 and C3 are evenly and symmetrically distributed to the gate fingers **32***a* and **29***a*, thereby enhancing the performance of the multi-gate FET structure **116**.

One skilled in the art would readily appreciate that the feedforward capacitor connection of the present invention is applicable to any FET structures and other electronic devices which require the use of feedforward capacitor(s). Such variations are contemplated as part of the present invention. Furthermore, in all these embodiments, the drain and source are interchangeable due to the symmetric placement of gates within a channel. Moreover, the layouts provided in these embodiments can be modified and scaled to include any number of serpentine gates, serpentine gate fingers, bussed gates, bussed gate fingers, drain fingers, source fingers, drain manifolds, source manifolds, feedforward capacitors, and/or cascaded FET structures as well as any width, length, thickness, size, shape and/or configuration for any component of the FET structures. In addition, these layouts can be modified and scaled to handle any FET device periphery and capacitor combination.

Additionally, while most of the embodiments presented herein relate to FET structures with integrally connected FET/feedforward capacitor structures, the invention is equally applicable to designs like that shown in FIG. **1B**, in which the capacitor and FET are not integrally coupled in the same structure, but are still electrically coupled. What is significant is the electrical connection formed between the gate and the capacitor metal layer of choice for harmonic power improvement. The importance of the connection lies in the reduction of the effect of distributed electrical resistance along the gate. The approaches outlined in this disclosure are intended to illustrate only a few of the many various alternatives for the gate connection to the feedforward capacitor and are not intended to be limiting. The invention is not limited to any specific type of connection to either the drain or the source, nor is it limited to use in designs in which the feedforward capacitor and FET are integral in one structure.

Even further, it is not necessary to the achievement of the desired effect that the bottom layer of the capacitor be the same structure as the gate manifold or that the top layer of the capacitor be the drain/source manifold of the FET.

It should be understood that the description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, and various changes and modifications within the spirit and scope of the invention as apparent to those skilled in the art are contemplated as part of the present invention.

What is claimed is:

1. A structure comprising:

a field effect transistor (FET) including a gate having a plurality of gate fingers, a plurality of source fingers, and a plurality of drain fingers; and

a feedforward capacitor integrally coupled with the FET for evenly or symmetrically distributing capacitance of the feedforward capacitor to the gate fingers, wherein the gate is a serpentine gate serpentining between the source and drain fingers, and includes first and second ends that are connected directly to the feedforward capacitor.

2. The structure of claim **1**, wherein the serpentine gate includes a middle portion that is not connected directly to the feedforward capacitor.

3. The structure of claim **1**, wherein the serpentine gate includes a middle portion that is also connected directly to the feedforward capacitor.

4. The structure of claim **1**, wherein the serpentine gate includes evenly distributed portions between the first and second ends, said evenly distributed portions being directly connected to the feedforward capacitor.

5. The structure of claim **1**, wherein the gate is a serpentine gate serpentining between the source and drain fingers, and includes first and second ends and at least one portion between the first and second ends, wherein said at least one portion and not the first and second ends is connected directly to the feedforward capacitor.

6. The structure of claim **5**, wherein said at least one portion of the serpentine gate is a middle portion of the

serpentine gate, or evenly distributed portions disposed between the first and second ends of the serpentine gate.

7. The structure of claim 1, wherein the gate is a bussed gate wherein each of the plurality of gate fingers is connected directly to the feedforward capacitor.

8. The structure of claim 1, wherein the feedforward capacitor includes a bottom conductive layer, a top conductive layer, and a dielectric layer disposed between the top and bottom conductive layers.

9. The structure of claim 8, wherein the gate fingers extend from the bottom conductive layer of the feedforward capacitor, and the drain or source fingers extend from the top conductive layer of the feedforward capacitor.

10. The structure of claim 1, further comprising:

a second FET including a second gate having a plurality of second gate fingers, a plurality of second source fingers, and a plurality of second drain fingers;

a second feedforward capacitor integrally coupled with the second FET for evenly or symmetrically distributing capacitance of the second feedforward capacitor to the second gate fingers; and

at least one third FET connected between the first and second FETs and including a third gate having a plurality of third gate fingers, a plurality of third source fingers, and a plurality of third drain fingers.

11. The structure of claim 10, wherein at least one of the first and second gates is a serpentine gate having first and second ends, the first and second ends of the serpentine gate being connected directly to the first or second feedforward capacitor.

12. The structure of claim 11, wherein the third gate is a serpentine gate, and the first, second and third FETs are connected in series with each other.

13. The structure of claim 12, wherein the serpentine gate includes a middle portion that is not connected directly to the first or second feedforward capacitor.

14. The structure of claim 12, wherein the serpentine gate includes a middle portion that is connected directly to the first or second feedforward capacitor.

15. The structure of claim 12, wherein the serpentine gate further includes evenly distributed portions between the first and second ends, said evenly distributed portions being directly connected to the feedforward capacitor.

16. The structure of claim 10, wherein at least one of the first and second gates is a serpentine gate having first and second ends and at least one portion between the first and second ends, wherein said at least one portion and not the first and second ends is connected directly to the first or second feedforward capacitor.

17. The structure of claim 16, wherein said at least one portion of the serpentine gate is a middle portion of the serpentine gate, or evenly-distributed portions disposed between the first and second ends of the serpentine gate.

18. The structure of claim 10, wherein at least one of the first and second gates is a bussed gate having a plurality of bussed gate fingers that are connected directly to the first or second feedforward capacitor.

19. The structure of claim 1, wherein:

the gate is a bussed gate having the plurality of gate fingers connected directly to the feedforward capacitor, and

wherein the structure further comprises at least one second gate having a plurality of second gate fingers serpentining between the source and drain fingers of the FET.

20. The structure of claim 19, wherein the feedforward capacitor is connected directly to a first side of the FET, and wherein the structure further comprises:

a third gate having a plurality of third gate fingers; and

a second feedforward capacitor integrally coupled to a second side of the FET for evenly or symmetrically distributing capacitance of the second feedforward capacitor to the third gate fingers.

21. The structure of claim 20, wherein the second and third gates are bussed gates having bussed gate fingers.

22. The structure of claim 20, wherein the first and second sides of the FET are drain and source sides respectively, or source and drain sides respectively.

23. The structure of claim 22, wherein one gate finger of the first gate, one gate finger of each of said at least one second gate, and one gate finger of the third gate are disposed between one of the source fingers and one of the drain fingers of the FET.

* * * * *

Microwave FET tutorial

Updated February 25, 2004

Welcome to the best web page on microwave FETs! This tutorial will provide an "outstanding understanding" of FETs as they are applied in microwave engineering; all of this information is directly applicable to understanding monolithic microwave integrated circuits (MMICs).

We are putting this important chapter of Microwaves101 onto the site in several installments because this topic is so huge in microwave engineering. The first installment is up and running as of Summer of 2003, and includes basic theory, all the terminology you will ever need, how FETs are made, and a discussion of I-V and transfer curves. Future installments will describe bias networks, including self-biasing analysis, small-signal modeling, FET power handling, and a large-signal discussion including drain efficiency, power-added efficiency, and load line analysis using the method first described by Steve Cripps. It is truly amazing how many brilliant microwave guys are named Steve. Contact us if there is any specific info we've omitted that you'd like to see here!

Here is a clickable table of contents for this page:

FET basics

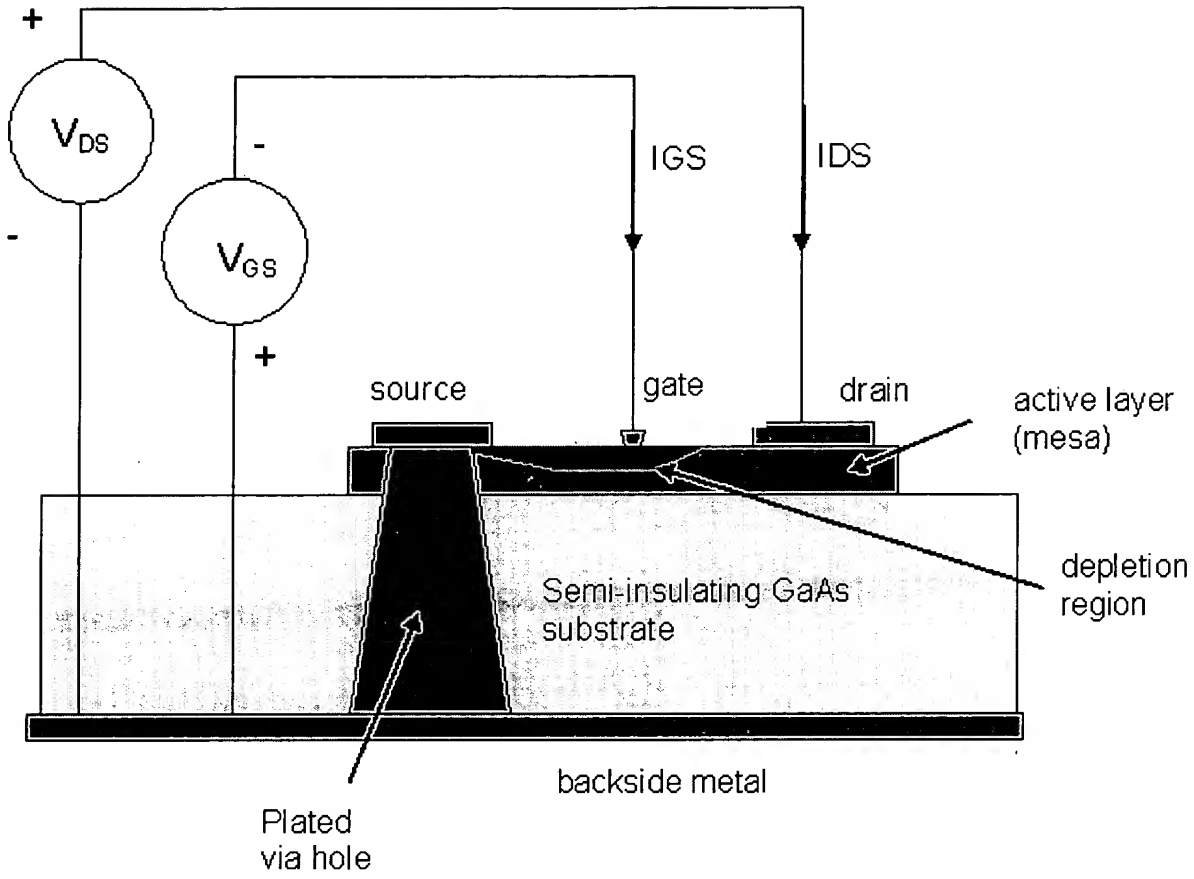
What's a FET? In microwaves we are almost always referring to a MESFET, which stands for metal-semiconductor field effect transistor. A FET is a three terminal device capable of both microwave amplification and switching. The FET's three terminals are denoted as gate, source and

drain. With respect to a bipolar transistor (BJT), the gate of a FET corresponds to the base of a BJT, the drain corresponds to the collector and the source corresponds to the emitter terminal. This is useful knowledge since every curve tracer we've ever seen in a lab has its three terminals labeled collector, base, and emitter, not drain, gate, and source. Pay attention, in case your boss puts you on the spot someday!

Used as an amplifier, the gate is most often configured as the input terminal, the source is grounded and the drain is the output. The output current (IDS) is controlled by the input voltage (VGS). This configuration is called common source since the source is common to the input and output ground connections. It is also possible (but unusual) to ground the gate and create a common-gate amplifier. Such an amplifier does not provide the voltage gain of the common-source amplifier, but it has the interesting property of being easier to impedance match than a "normal" common-source amplifier. We won't get into that here.

The figure below shows a cross-section of the channel of a field-effect transistor and explains some FET terminology. The drain and source are connected by the FET channel, which is formed by creating a mesa of N-type semiconductor (for an N-channel FET) on top of a semi-insulating substrate (typically GaAs). In microwaves we are almost often dealing with N-channel FETs. P-channel FETs are possible but are never used at microwave frequencies, because they would have far worse performance compared to N-channel FETs. Go ask a device guy why that is and he will explain to you something about the electron mobility of the device, but who really cares? The drain and source contacts are connected to the channel with ohmic metal contacts that form low-resistance connections to these terminals. The gate connection to the channel is formed between the drain and source by a Schottky metal contact to the channel. The rectifying property of the gate contact means that when it is reverse biased with respect to the channel it conducts almost zero DC current (IGS) to the channel, but its electric field can be used to effectively displace the electrons within the channel. Thus an AC voltage incident on the gate terminal causes a variable resistance between the source and drain of the FET. When the gate reaches pinch-off voltage the electrons below the gate are depleted to the point where essentially no current can flow from drain to source.

The source connection is the "source" of electrons in the channel, and the drain is where they are "drained off". Remember that we are talking about electrons flowing here, and you will see that the direction of current flow is positive from drain to source.



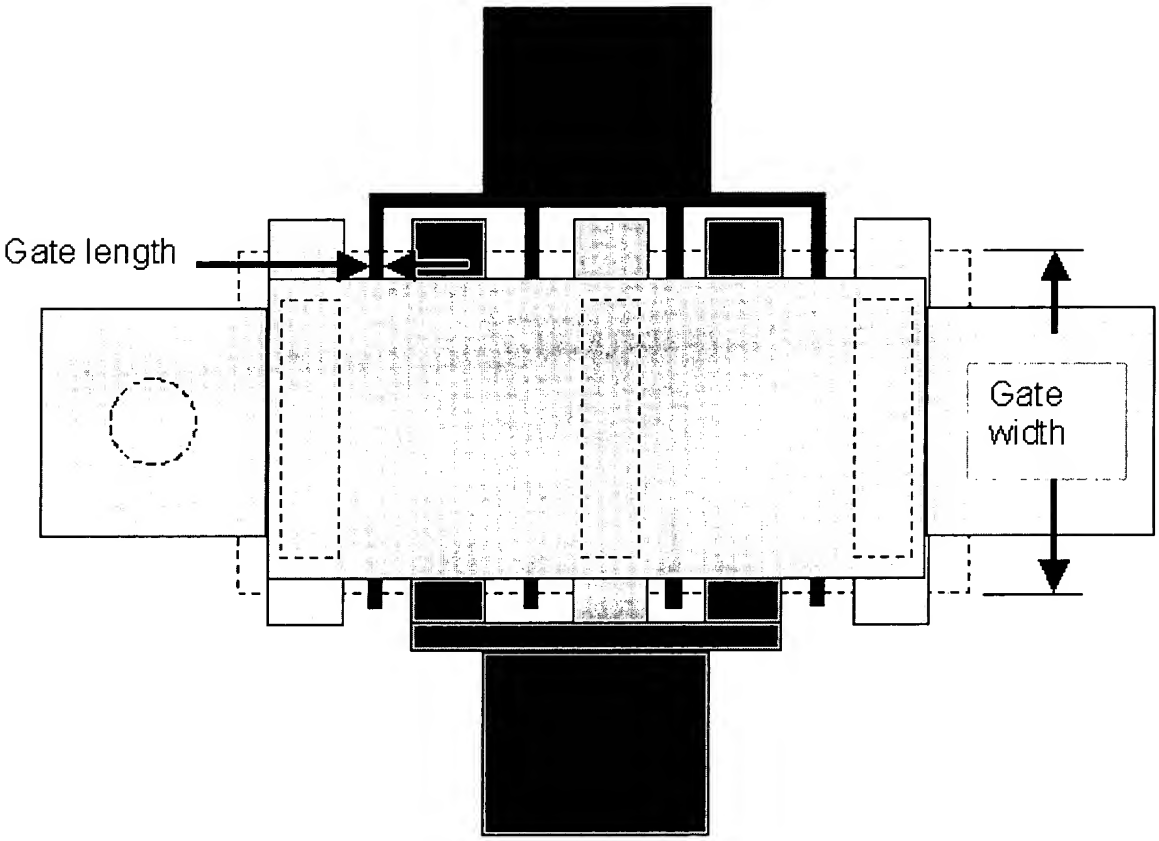
FET geometry lesson

FET geometry refers to the physical dimensions of a FET. FET dimensions are always described in microns or millimeters, never in mils, with the exception that overall chip dimensions (length, width and thickness) as often given in mils as well as microns. This is because the next higher assembly (artwork for a thin-film network for example) is often dimensioned in inches.

Gate length is often confused with **gate width**. Just remember when you look at a gate finger, gate *length* is the short dimension and gate *width* is the long dimension. This is illustrated in the figure below. Gate length has a major effect on maximum frequency of operation: one-micron gates start to suck wind at C-band, half-micron gates are good through X-band, quarter-micron gates are good into Ka-band, and 0.15 micron gates can work up through W-band. What is the limit on gate length? We aren't there yet, some companies are experimenting with 50 to 100 *nanometer* gates!

Gate width refers to the unit width of the gate as it passes between the

source and drain across the mesa (the semiconducting area of a FET). Wider gates mean more DC and RF current, and therefore more power capability. Gate width must be sized appropriate to frequency: if the gate width starts to become an appreciable fraction of a wavelength, the RF performance of the FET starts to suffer. At X-band, power FETs often have 150 um wide gates. At Ka band the the gate width is typically 75 micron maximum. At W-band perhaps 40 micron fingers is the upper limit.

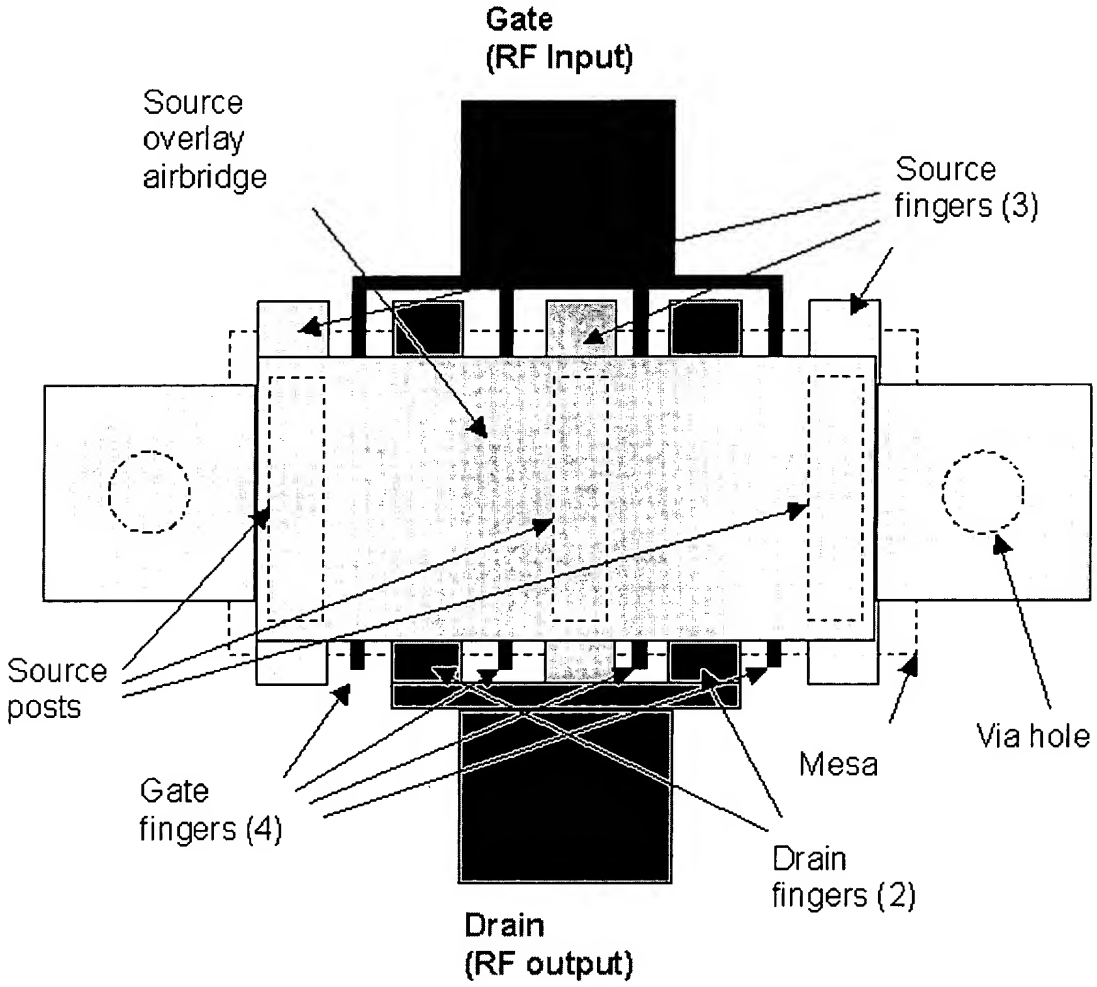


A **gate finger** refers to a single gate structure. **Gate periphery** is the total size of a FET. Most FETs have multiple gate fingers, so the periphery is equal to the number of gate fingers times the unit gate width. In the example figure there are four gate fingers. Many of the FET parameters can be directly scaled with gate periphery, for example the saturated drain current is proportional to gate periphery.

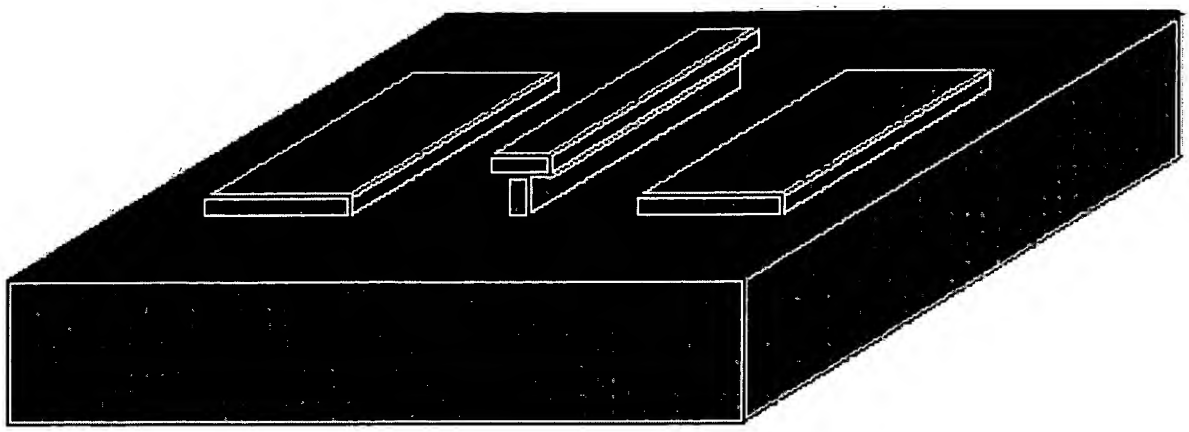
The **gate bus-bar** is the electrical contact that is used to connect all of the multiple gate fingers together. The **drain bus bar** serves a similar purpose.

Via holes are what connect the source (or individual sources) to the chip backside metal, which is considered RF and DC ground. When individual

sources are grounded with separate via holes, these vias are referred to as **ISVs** which stands for individual source vias. ISVs are only used on very thin FETs, perhaps with two mils (50 microns) maximum thickness. ISVs provide very low-inductance grounding to the source connection, providing the most gain and efficiency for power amplifiers, which becomes more important for power FETs operating at millimeter-wave frequencies. On four-mil GaAs and thicker, ISVs are not usually possible, because the source contact pad is typically smaller than the minimum diameter of an etched via hole.



Mushroom gate or **tee gate** refers to a technique of providing very short effective gate length, while providing low gate resistance. **Gate resistance** is a parasitic element that affects the maximum available gain of a FET, and is inversely proportional to the cross-sectional area of metal along the gate finger. A picture of a tee-gate is shown below. This type of structure involves extra process steps and is therefore used only in higher-frequency applications where short gates are required, such as X-band through millimeter-waves.



Answers to FET FAQs:

Why use GaAs?

The FET is built on top of a semi-insulating substrate, most often GaAs. When we say "semi-insulating" this is perhaps misleading. In its pure form, GaAs is remarkable insulator, which is what makes monolithic microwave integrated circuits (MMICs) practical. Here is one advantage GaAs has over silicon. Pure silicon is a better conductor than pure GaAs, so it tends to dissipate electrical fields that are needed to support transmission modes and hence needs some "help" to be used as a MMIC. We'll discuss that later.

What's a compound semiconductor?

GaAs is referred to as a "compound semiconductor", because it is a crystal of more than one element. Silicon is a semiconductor all by itself. GaAs wafers are available in up to six inch diameter, but more often FET and MMIC manufacturers use four-inch material.

What does III-V semiconductor refer to?

Three-five material refers to compound semiconductors made from one element from Group III on the periodic chart (arsenic in the case of GaAs) and one from Group V (gallium in the case of GaAs). Other three-five (or III-V in Roman numerals) semiconductors include indium phosphide and gallium nitride. TriQuint Semiconductor derived their name from the III-V material that their business is based on (GaAs, of course!)

Are FETs toxic waste?

The short answer is "yes", although I have seen a person eat a MMIC and live just to prove this wrong. Gallium arsenide may not kill you, but it has a nasty habit of breaking down into gallium and arsenide if left in your town dump or incinerator. Traces of arsenide in water cause cancer, while small doses are quite lethal. Remember the play "Arsenic and Old Lace"?

In the United states the GaAs industry has strict controls on what they can flush into the wastewater stream. Even though they saw, etch, and polish tons of GaAs wafers each year, GaAs foundries have some clever ways of separating out the bad stuff before it goes down the drain, so give them credit for being good citizens.

The EPA's specification on arsenic in drinking water is 50 parts per *billion*. Check out your water bill next month, we often go over this limit. Could it be the 130 million cell phones (65,000 tons) that get discarded every year are putting us over the top? Damn right, and wireless trash contributes a plethora of poisonous substances to your community, associated with cancer and a range of reproductive, neurological and developmental disorders, including:

- Metals such as arsenic, antimony, beryllium, cadmium, copper, lead, nickel and zinc ,
- Brominated flame retardants,
- Dioxins and furans (produced during incineration).

We predict that someday your wireless service provider will have to take care of safely disposing your obsolete or broken phone equipment. Until then it's your responsibility. One option is to check out Charitable Recycling, a U.S. charitable organization (duh) that pays a dollar to charity for every unwanted cell phone turned in. Then they fix up the phones and donate them to needy people all over the world. Hopefully these needy people don't burn your little gift to keep their mud hut warm! You can go to their site for information about local collection sites and the charities they support. Perhaps a better option is the Rechargeable Battery Recycling program available at many places where you buy batteries (like Sears, Home Depot, Ace Hardware and Radio Shack).

What does "bandgap" refer to?

Bandgap is a material property that takes some knowledge of semiconductor physics to understand. Who cares? You might. The higher the bandgap, the higher the breakdown voltage the material can support. High breakdown is a huge advantage for power amplifiers, remember Ohm's law and you will see that voltage swing is proportional to power. GaAs is a medium bandgap technology at 1.5 electron-volts, you can get

20 volts breakdown on a good day with a GaAs MESFET. InP is a low-bandgap device at 0.75 electron-volts, it only supports a few volts breakdown. The "great white hope" (is that politically incorrect or what?) of microwave semiconductors is gallium nitride, which is a wide bandgap semiconductor at greater than 3 electron-volts bandgap energy. GaN FETs have exhibited over 100 volts breakdown voltage. DARPA is a big fan of GaN technology and is spending tens of millions of taxpayer dollars trying to develop this technology beyond a laboratory curiosity that blows up in a few hours of operation into the "next big thing" for solid-state microwave power.

What is the difference between Schottky and Ohmic contacts?

What is a Schottky contact? It is a diode junction formed between certain metals and semiconductors. You can read about the illustrious Mr. Schottky here. Metals that form Schottky contacts to N-type GaAs include aluminum, gold, silver, titanium and platinum. Often an alloy of metals is used in FETs, such as titanium/platinum/gold (Ti/Pt/Au).

The drain and source contacts are considered "ohmic" because they behave resistively, that is, they pass current in either direction obeying Ohm's law where current is proportional to voltage. The ohmic metal is usually the first layer of metal applied when a FET or a MMIC is fabricated.

What does semiconductor refer to?

Based on differences in bulk resistivity, five classes of materials are in common usage, namely conductors, semiconductors, semi-insulators, insulators and super-conductors. There is no IEEE standard for these categories, and if someone can supply a good reference on this point we'd appreciate it! Click here for the Microwaves101 version of the definition of these categories.

GaAs bulk resistvity can be tailored over a huge range, 10^{-6} to 10^{22}, so that GaAs can be anywhere from a conductor to an insulator. By doping Chrome is usually added to the melt to raise resistivity, but this trick has its limitations (it does not stay stable through wafer processing steps). High purity, undoped GaAs can be 10^{7} to 10^{8} ohm-cm.

Intrinsic versus extrinsic GaAs ? intrinsic refers to the pure crystal, extrinsic refers to the doped material where conduction is due to donor or acceptors.

Thermal conductivity of FETs

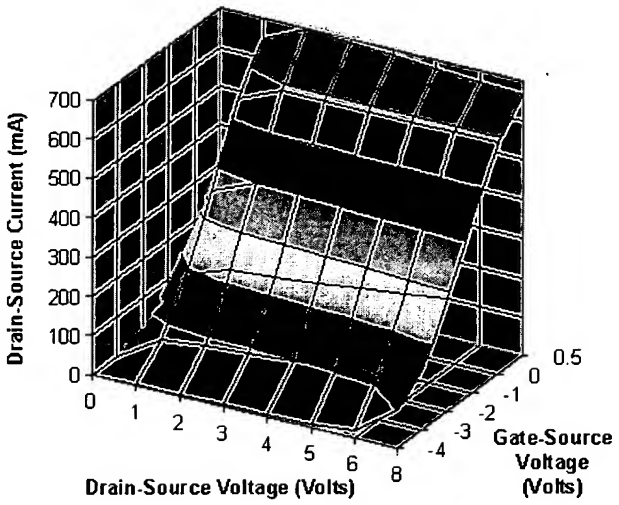
The thermal conductivity (TC) of GaAs varies at 1/T (T in Kelvin). It is approximately 0.55 W/cmC at room temperature.

How FETs and MMICs are made

This discussion got so big we had to put it on a separate page! Click here to check out our latest description of microwave semiconductor processing.

FET IV and Transfer Curves

The operation of any three-terminal device is well described on a three dimensional surface plot as shown below. For an FET, the output characteristics VDS and IDS are shown to be a function of the input voltage VGS. A typical FET response is shown below.



Three-dimensional FET IV characteristics

The three-dimensional characteristics are most often collapsed onto a 2-D plot of IV curves, as shown below. Here the output drain current/voltage relationship is plotted at discrete gate voltage. Such a plot can be produced from a FET using any Tektronics curve tracer. Depicted on this plot are some definitions:

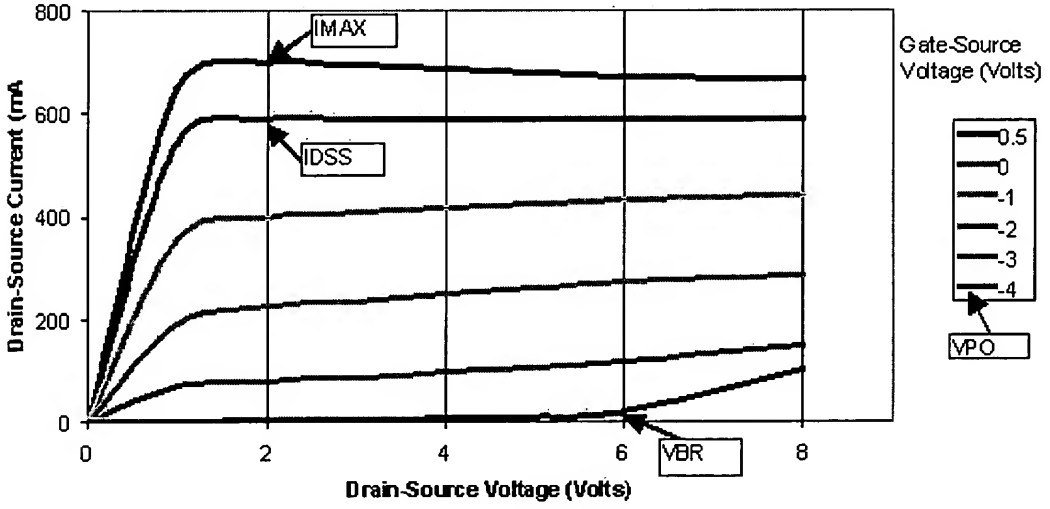
IMAX: the drain-source current when the gate is forward biased for maximum channel current. This is typically measured at +0.5 volts on the gate (higher potentials will merely start to conduct current across the gate Schottky contact which tends to roast your FET) and perhaps 1.5 or 2 Volts drain-to-source.

IDSS: the saturated drain-source current when the gate is biased at zero volts (grounded to the source). This is typically measured at 1.5 or 2 Volts drain-to-source.

VPO: pinch-off voltage. This is where the drain-source terminals start to look like an open circuit, and no appreciable current flows even at high drain-source potentials. In practice there is always some residual current and the actual VPO measurement must make an allowance for this. For example, the pinch-off voltage could be measured at 2.5% of IDSS and VDS=2 volts.

VBR: the gate-source breakdown voltage, which is indirectly measured on the IV curves. At high drain-source potential and near pinch-off, the IV curves tend to bend up. As shown in the picture the breakdown voltage VGS is approximately 10 volts (VGS=-4 volts and VDS=6 volts combined).

Knee voltage: the voltage at which the curves transition from "linear" to "saturation". In the linear region, IDS depends on both VGS and VDS (from VDS=0 Volts to approximately VDS=2 Volts). In the saturation region, IDS depends mainly on VGS and not VDS. This is the right side of the curve, beyond VDS=2 volts..

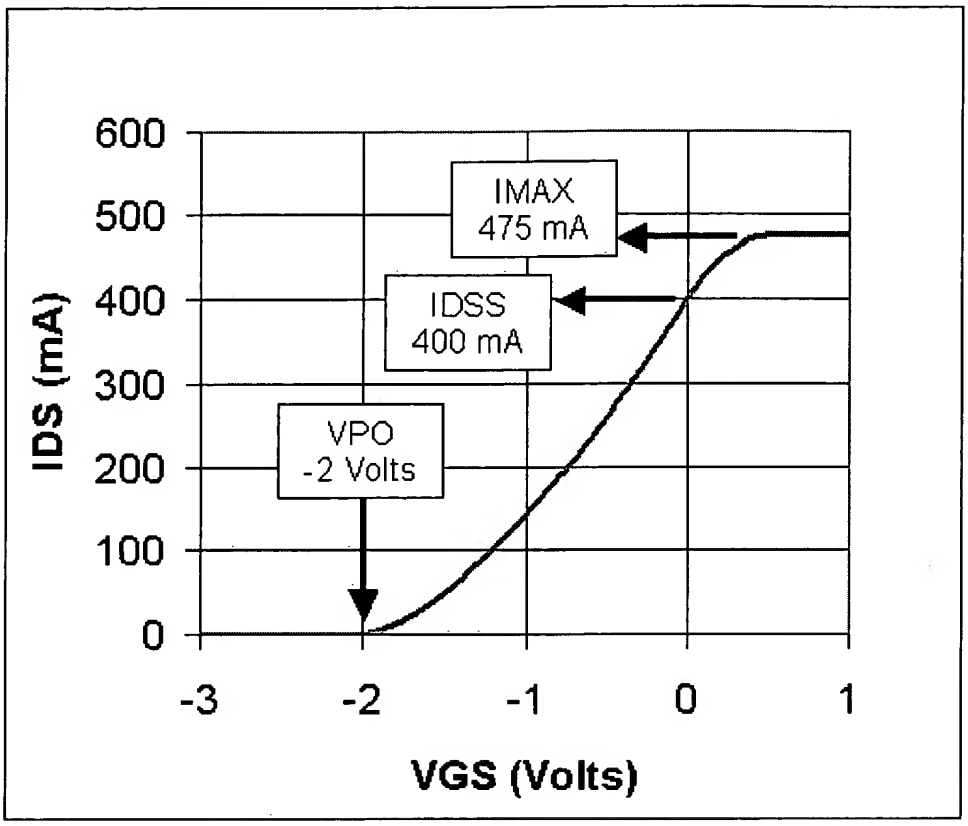


FET

IV characteristics and definitions

Another very useful plot of the FET's characteristics is called the FET transfer characteristic. Here we see the variation in drain voltage due to variation in gate voltage, at some fixed drain voltage in the saturation region (beyond VDS=2 Volts). This is analogous to looking at a cut in the Y-Z plane in the surface plot above. Plotted below is the transfer characteristic of a FET. This type of plot is extremely useful in designing self-biasing networks which are described below. Here we see why a FET

is an effective amplifier: for a quiescent point of –1 Volts, a peak-to-peak voltage swing of +/-0.5 Volts on the gate terminal provides a variation in drain current from 50 to 250 mA.



FET Transfer Characteristics

Where did we get the nice transfer curve shown in the above plot? We have developed a model that allows the user to fit a continuous transfer curve to measured data, with separate coefficients to fit the regions above and below VGS=0 Volts. The equations are shown below. By using two different exponent terms, is possible to control the ratio of IMAX/IDSS, which is impossible in simpler models. Soon we will put a spreadsheet in the download area that contains these equations for you to use when fitting your own FET. Check back in June 2003. By the way, the third equation is missing a minus sign. Find it and you've won a pen knife!

$$I_{DS} = 0 \quad for \quad V_{GS} < V_{PO}$$

$$I_{DS} = I_{DSS} \times \left(1 - \frac{V_{GS}}{V_{PO}}\right)^{EXP1} \quad for \quad V_{PO} < V_{GS} \leq 0$$

$$I_{DS} = I_{DSS} \times \left(1 - \frac{EXP1 \cdot V_{MAX}}{V_{PO} \cdot (EXP2 + 1)}\right) + I_{DSS} \times \frac{EXP1 \cdot V_{MAX}}{V_{PO} \cdot (EXP2 + 1)} \times \left(1 + \frac{V_{GS}}{V_{MAX}}\right)^{(EXP2+1)} \quad for \quad 0 < V_{GS} \leq V_{MA}$$

$$I_{DS} = I_{MAX} = I_{DSS} \times \left(1 - \frac{EXP1 \cdot V_{MAX}}{V_{PO} \cdot (EXP2 + 1)}\right) \quad for \quad V_{GS} \geq V_{MAX}$$

Types of microwave FETs

With respect to their intended operation, FETs can be divided into three categories: low noise, power and switch FETs. Low noise FETs are optimized to provide the lowest possible noise figure at very low voltage and power (perhaps 1.5 volts and 10 ma). Power FETs possess higher breakdown voltage than low noise FETs and can therefore operate at higher voltages, and are much larger in periphery than low noise FETs. Switching FETs are intended to operate passively (no drain current and no gain); the gate voltage is merely used to switch the device from a resistive element to a small capacitive element. Switch FETs can be configured in series with a transmission line (drain and source act as input or output), or in shunt, with the source grounded.

A "depletion mode" FET is one where the gate is mainly used to reduce the current within the channel (most common microwave FETs are depletion mode). An "enhancement mode" FET does not conduct drain-to-source until the gate is slightly forward biased. Think of this as a depletion-mode FET with a zero-volt pinch-off voltage. There is a big limitation to enhancement-mode FETs: you can't exceed the turn-on voltage of the Schottky contact, which is typically 0.7 volts, so the gate etching process has to be well-controlled to produce a FET with pinch-off of zero volts or perhaps a few tenths of a positive volt. Etch too far and you will end up with no FET at all, just a capacitor between drain and source!

FET bias networks

Bias networks are what are used to put a FET at the intended **quiescent operating point**. For example, you might want to operate a FET in a power amplifier at 6 volts VDS and at 50% of the saturated drain current (IDSS/2). This is the quiescent point.

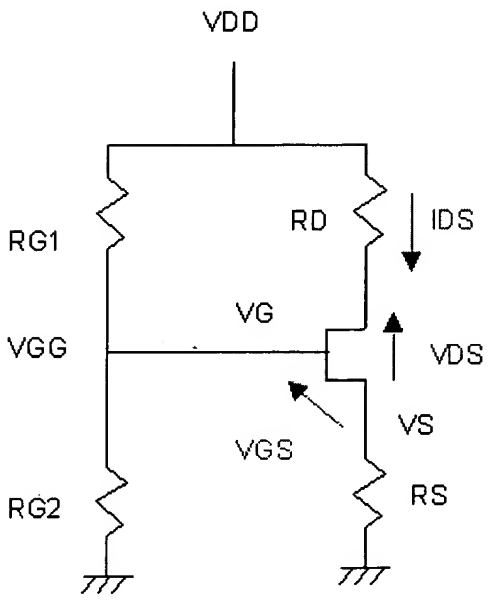
You might want to see our definition of a "bias tee" in our page on microwave filters.

FET DC characteristics, such as IDSS and VPO vary from lot to lot, and even within a wafer. This complicates the life of the amplifier designer, since VGS needs to be set to achieve either a fixed fraction of the saturated drain current, or a fixed current. One amplifier might need VGS to be –1.05 volts, another might need VGS =-2.1 volts to perform as designed. What's a designer to do?

There are at least three ways to bias up a FET amplifier to get to the intended quiescent operating point. The most obvious is to have separate DC power supplies for the gate and drain connections, with the gate supply being adjustable, and ground the source. Grounding the source directly will provide the most gain from the FET, which is why this is a good idea if efficiency is a concern. In practice, the "adjustable" gate bias supply is often a fixed supply of perhaps –5 Volts, with an adjustable resistor-divider network being employed to supply the needed gate voltage.

Another method of biasing a FET is with an **active bias** network. This is an analog circuit that attempts to eliminate any manual adjustments to the FET Q-point, by using a small FET to "calculate" the required gate bias for the FET in the circuit and supply it to the larger FET which is the active device in the amplifier. Such a circuit is often called a "current mirror" and won't be covered here at this time. (Wanna contribute on this topic, Mr. Studley Power Amp Designer? Contact us!) An active bias network, if designed properly, does not reduce the overall efficiency of a power amplifier by much. However, a negative supply voltage is still required, although it need only be at a fixed voltage such as –5 Volts.

The third way to bias a FET is to employ a **"self-biasing"** network, in which a resistor of a strategic value is placed between the source connection and ground. The resistor is bypassed with a capacitor so that the FET source connection sees a zero-Ohm connection to ground at the operating frequency. When drain current flows through the FET and then through the source resistor, the source voltage rises above ground. The gate voltage is either held at a fixed voltage or grounded, resulting in a fixed negative gate-source voltage, which is (hopefully) the intended Q-point. For example, if the gate was grounded, and the FET was drawing 200 ma of drain current through a 10-ohm source resistor, the gate-source bias would be –2 volts. The major advantage of the self-bias scheme over other bias schemes is that only a single positive voltage supply is needed to power up the amplifier. The down-sides to using self-bias schemes are that amplifier efficiency is lost due to the voltage drop of the source resistor. Also, the FET cannot be RF grounded at all frequencies as well as if it was DC grounded with via holes, so gain and efficiency can be degraded as a result. Self-bias networks are often used in LNAs, but not power amplifiers, for these two reasons.



Self-bias network with raised gate voltage

Self-biasing secrets

The self-bias network is used to eliminate the need for a negative voltage to a FET-based amplifier. One of the ways to make a design less susceptible to normal variations in FET transfer characteristics (the gate voltage needed to induce a fixed drain current) is to raise the gate bias above ground. Such designs are often called "raised gate bias" designs. Duh! Below we will prove to you that raised gate bias designs are advantageous in this regard. We also will supply you with an Excel spreadsheet where you can analyze your particular design to make it immune to variations in pinch-off voltage and IDSS.

While you are waiting for us to provide you with a self-biasing spreadsheet, check out this spreadsheet available on the website of St. Louis Community College. Thanks, Frederick!

The self-biasing analysis is coming soon!

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